WHAT IS CLAIMED IS:

1. An erasing method for non-volatile memory, wherein the non-volatile memory has a gate, a source, a drain, an electron-trapping layer and a substrate, the erasing method comprising the steps of:

applying a first voltage to the gate, applying a second voltage to the source, applying a third voltage to the drain and applying a fourth voltage to the substrate so that electrons are pulled out from the electron-trapping layer into the channel of a memory cell utilizing a negative gate F-N tunneling effect in an erasing operation.

2. The erasing method of claim 1, wherein the non-volatile memory is a two bits per cell type of memory or a one bit per cell type of memory.

3. The erasing method of claim 1, wherein the control gate is an N-type gate or a P-type gate.

4. The erasing method of claim 1, wherein the electron-trapping layer contains net negative charges while stationed in the erased state and the operation involves only electron transfer.

5. The erasing method of claim 1, wherein the voltage difference between the first voltage applied to the gate and the fourth voltage applied to the substrate is sufficient to trigger erasing the data from the non-volatile memory through negative gate F-N tunneling effect.

6. The erasing method of claim 1, wherein the voltage difference between the first voltage applied to the gate and the fourth voltage applied to the substrate is between about –10V to –20V.

7. The erasing method of claim 6, wherein the first voltage is set to a value between about –10V to –20V.

8. The erasing method of claim 7, wherein the fourth voltage is set to a value between about 0V to 10V.

9. The erasing method of claim 1, wherein the second voltage applied to the source, the third voltage applied to the drain and the fourth voltage applied to the substrate has identical value so that very few holes are produced within the substrate to cause substantial stress.

10. The erasing method of claim 9, wherein the second voltage, the third voltage and the fourth voltage are set to values between about 0V to 10V.

11. The erasing method of claim 10, wherein the first voltage is set to a value between about –10V to –20V.

12. An operating method for a non-volatile memory, wherein the non-volatile memory includes a gate, a source, a drain, an electron-trapping layer and a substrate, the operating method comprising the steps of:

programming the non-volatile memory to a programmed threshold voltage Vt_P; and

setting the non-volatile memory to an erased threshold voltage Vt_E by applying a first voltage to the gate, applying a second voltage to the drain, applying a third voltage to the source and applying a fourth voltage to the substrate so that electrons are pulled out from the electron-trapping layer into the channel of a memory cell utilizing a negative gate F-N tunneling effect in an erasing operation.

13. The operating method of claim 12, wherein the non-volatile memory is a two bits per cell type of memory or a one bit per cell type of memory.

14. The operating method of claim 12, wherein the control gate is an N-type gate or a P-type gate.

15. The operating method of claim 12, wherein the step of programming the memory cell of a non-volatile memory to a programmed threshold voltage Vt_P includes using a channel hot electron method.

16. The operating method of claim 12, wherein before the step of programming the memory cell of the non-volatile memory to the programmed threshold voltage Vt_P further includes conducting an initialization step.

17. The operating method of claim 16, wherein the initialization step includes utilizing F-N tunneling effect to increase the threshold voltage of a memory cell from an initial threshold voltage Vti to an erased threshold voltage Vt_E.

18. The operating method of claim 16, wherein the initialization step may further includes the sub-steps of:

programming a memory cell of the non-volatile memory so that the threshold voltage of the memory cell rises from an initial threshold voltage Vti to a programmed threshold voltage Vt_P; and

lowering the threshold voltage of the memory cell from the programmed threshold voltage Vt_P to an erased threshold voltage Vt_E utilizing negative gate F-N tunneling effect.

19. The operating method of claim 18, wherein the erased threshold voltage Vt_E is greater than or equal to the initial threshold voltage Vti.

20. The operating method of claim 19, wherein the fact that the erased threshold voltage Vt_E is greater than or equal to the initial threshold voltage Vti indicates that the

electron-trapping layer still contains an excess of negative charges in the erased state and the operation involves only electron transfer.

21. The operating method of claim 12, wherein the voltage difference between the first voltage applied to the gate and the fourth voltage applied to the substrate is between about –10V to –20V.

22. The operating method of claim 21, wherein the first voltage is set to a value between about –10V to –20V.

23. The operating method of claim 21, wherein the fourth voltage is set to a value between about 0V to 10V.

24. The operating method of claim 12, wherein the second voltage applied to the source, the third voltage applied to the drain and the fourth voltage applied to the substrate has identical value so that very few holes are produced within the substrate to cause substantial stress.

25. The operating method of claim 24, wherein the second voltage, the third voltage and the fourth voltage are set to values between about 0V to 10V.

26. The operating method of claim 25, wherein the first voltage is set to a value between about –10V to –20V.